

IN THE CLAIMS:

No claim amendments are proposed by Applicants in this response.

1 1. (Previously Presented) A computer implemented method comprising:
2 requesting a first deferred procedure call for a first interrupt event associated with a
3 source;
4 requesting at least one other different deferred procedure call for a second interrupt event
5 associated with the source, wherein the first interrupt event comprises one type of
6 event and the second interrupt event comprises another type of event;
7 assigning the first deferred procedure call and the at least one other deferred procedure
8 call to a resource;
9 processing the first interrupt event with the first deferred procedure call; and
10 processing the second interrupt event with the at least one other deferred procedure call.

1 2. (Original) The method of claim 1, further comprising:
2 assigning the first deferred procedure call and the at least one other deferred procedure
3 call to a resource comprising a processor exhibiting a single thread of execution;
4 and
5 executing the first deferred procedure call and the at least one other deferred procedure
6 call on the single thread.

1 3. (Original) The method of claim 1, further comprising:
2 assigning the first deferred procedure call and the at least one other deferred procedure
3 call to a resource comprising a processor exhibiting a plurality of threads; and
4 executing the first deferred procedure call on one thread of the plurality of threads while
5 executing the at least one other deferred procedure call on another thread of the
6 plurality of threads.

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1 4. (Original) The method of claim 1, further comprising:
2 assigning the first deferred procedure call to a resource comprising a first thread of a
3 processor;
4 assigning the at least one other deferred procedure call to a resource comprising a second
5 thread of the processor; and
6 executing the first deferred procedure call on the first thread while executing the at least
7 one other deferred procedure call on the second thread.

1 5. (Original) The method of claim 1, further comprising:
2 assigning the first deferred procedure call and the at least one other deferred procedure
3 call to a resource comprising a multi-processor system; and
4 executing the first deferred procedure call on one processor of the multi-processor system
5 while executing the at least one other deferred procedure call on another processor
6 of the multi-processor system.

1 6. (Original) The method of claim 1, further comprising:
2 assigning the first deferred procedure call to a resource comprising a first processor;
3 assigning the at least one other deferred procedure call to a resource comprising a second
4 processor; and
5 executing the first deferred procedure call on the first processor while executing the at
6 least one other deferred procedure call on the second processor.

1 7. (Previously Presented) The method of claim 1, further comprising
2 processing a third interrupt event associated with the source with the first deferred
3 procedure call, the third interrupt event comprising a third type of event.

1 8. (Previously Presented) A computer implemented method comprising:
2 requesting a first deferred procedure call for a first interrupt event associated with a
3 source;
4 requesting at least one other different deferred procedure call for a second interrupt event
5 associated with the source, wherein the first interrupt event comprises one type of
6 event and the second interrupt event comprises another type of event; and
7 processing the first interrupt event with the first deferred procedure call while processing
8 the second interrupt event with the at least one other deferred procedure call.

1 9. (Original) The method of claim 8, further comprising:
2 executing the first deferred procedure call on a first thread of a processor; and
3 executing the at least one other deferred procedure call on a second thread of the
4 processor.

1 10. (Original) The method of claim 8, further comprising:
2 executing the first deferred procedure call on a first processor; and
3 executing the at least one other deferred procedure call on a second processor.

1 11. (Previously Presented) The method of claim 8, further comprising
2 processing a third interrupt event associated with the source with the first deferred
3 procedure call, the third interrupt event comprising a third type of event.

1 12. (Previously Presented) A driver comprising:
2 an interrupt handler to identify interrupt events associated with a source;
3 a first deferred procedure call, the first deferred procedure call to process a first type of
4 the interrupt events; and
5 a second different deferred procedure call, the second deferred procedure call to process a
6 second type of the interrupt events.

1 13. (Previously Presented) The driver of claim 12, the interrupt handler to
2 assign the first and second deferred procedure calls to a resource for execution.

1 14. (Previously Presented) The driver of claim 12, the interrupt handler to
2 assign the first deferred procedure call to a first resource for execution and the second
3 deferred procedure call to a second resource for execution.

1 15. (Previously Presented) A computer system comprising:
2 a driver stored in a memory of the computer system, the driver including
3 an interrupt handler to identify interrupt events associated with a source;
4 a first deferred procedure call, the first deferred procedure call to process a first
5 type of the interrupt events; and
6 a second different deferred procedure call, the second deferred procedure call to
7 process a second type of the interrupt events;
8 and
9 a processor to execute the ~~the~~ first and second deferred procedure calls.

1 16. (Previously Presented) The computer system of claim 15, the interrupt
2 handler to assign the first and second deferred procedure calls to a single thread exhibited
3 by the processor for execution.

1 17. (Previously Presented) The computer system of claim 15, the interrupt
2 handler to assign the first deferred procedure call to one thread of the processor and the
3 second deferred procedure call to a second thread of the processor for execution.

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1 18. (Previously Presented) The computer system of claim 15, the interrupt
2 handler to assign the first deferred procedure call to the processor and the second deferred
3 procedure call to a second processor for execution.

1 19. (Previously Presented) The computer system of claim 15, wherein the
2 source comprises a peripheral device coupled with the computer system.

1 20. (Previously Presented) An article of manufacture comprising:
2 a machine accessible medium, the machine accessible medium providing instructions
3 that, when executed by a machine, cause the machine to:
4 request a first deferred procedure call for a first interrupt event associated with a
5 source;
6 request at least one other different deferred procedure call for a second interrupt
7 event associated with the source, wherein the first interrupt event
8 comprises one type of event and the second interrupt event comprises
9 another type of event;
10 assign the first deferred procedure call and the at least one other deferred
11 procedure call to a resource;
12 process the first interrupt event with the first deferred procedure call; and
13 process the second interrupt event with the at least one other deferred procedure
14 call.

1 21. (Original) The article of claim 20, wherein the instructions, when
2 executed, further cause the machine to:
3 assign the first deferred procedure call and the at least one other deferred procedure call
4 to a resource comprising a processor exhibiting a single thread of execution; and
5 execute the first deferred procedure call and the at least one other deferred procedure call
6 on the single thread.

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1 22. (Original) The article of claim 20, wherein the instructions, when
2 executed, further cause the machine to:
3 assign the first deferred procedure call and the at least one other deferred procedure call
4 to a resource comprising a processor exhibiting a plurality of threads; and
5 execute the first deferred procedure call on one thread of the plurality of threads while
6 executing the at least one other deferred procedure call on another thread of the
7 plurality of threads.

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1 23. (Previously Presented) The article of claim 20, wherein the instructions,
2 when executed, further cause the machine to:
3 assign the first deferred procedure call to a resource comprising a first thread of a
4 processor;
5 assign the at least one other deferred procedure call to a resource comprising a second
6 thread of the processor; and
7 execute the first deferred procedure call on the first thread while executing the at least
8 one other deferred procedure call on the second thread.

1 24. (Original) The article of claim 20, wherein the instructions, when
2 executed, further cause the machine to:
3 assign the first deferred procedure call and the at least one other deferred procedure call
4 to a resource comprising a multi-processor system; and
5 execute the first deferred procedure call on one processor of the multi-processor system
6 while executing the at least one other deferred procedure call on another processor
7 of the multi-processor system.

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1 25. (Original) The article of claim 20, wherein the instructions, when
2 executed, further cause the machine to:
3 assign the first deferred procedure call to a resource comprising a first processor;
4 assign the at least one other deferred procedure call to a resource comprising a second
5 processor; and
6 execute the first deferred procedure call on the first processor while executing the at least
7 one other deferred procedure call on the second processor.

1 26. (Previously Presented) The article of claim 20, wherein the instructions,
2 when executed, further cause the machine to process a third interrupt event associated
3 with the source with the first deferred procedure call, the third interrupt event comprising
4 a third type of event.

1 27. (Previously Presented) An article of manufacture comprising:
2 a machine accessible medium, the machine accessible medium providing instructions
3 that, when executed by a machine, cause the machine to:
4 request a first deferred procedure call for a first interrupt event associated with a
5 source;
6 request at least one other different deferred procedure call for a second interrupt
7 event associated with the source, wherein the first interrupt event
8 comprises one type of event and the second interrupt event comprises
9 another type of event; and
10 process the first interrupt event with the first deferred procedure call while
11 processing the second interrupt event with the at least one other deferred
12 procedure call.

1 28. (Original) The article of claim 27, wherein the instructions, when
2 executed, further cause the machine to:
3 execute the first deferred procedure call on a first thread of a processor; and
4 execute the at least one other deferred procedure call on a second thread of the processor.

1 29. (Original) The article of claim 27, wherein the instructions, when
2 executed, further cause the machine to:
3 execute the first deferred procedure call on a first processor; and
4 execute the at least one other deferred procedure call on a second processor.

1 30. (Previously Presented) The article of claim 27, wherein the instructions,
2 when executed, further cause the machine to process a third interrupt event associated
3 with the source with the first deferred procedure call, the third interrupt event comprising
4 a third type of event.

1 31. (Previously Presented) The method of claim 1, wherein the source
2 comprises a peripheral device of a computer system.

1 32. (Previously Presented) The method of claim 8, wherein the source
2 comprises a peripheral device of a computer system.

1 33. (Previously Presented) The driver of claim 12, wherein the source
2 comprises a peripheral device of a computer system.

1 34. (Previously Presented) The article of manufacture of claim 20, wherein
2 the source comprises a peripheral device of a computer system.

1 35. (Previously Presented) The article of manufacture of claim 27, wherein
2 the source comprises a peripheral device of a computer system.